DETAILED ACTION

Response to Amendment

The amendment filed on July 15, 2011 has been received and entered.

Applicant's Amendments to the Claims have been received and acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stallkamp US Patent No. 6,895,009 B1 (hereinafter Stallkamp) in view of Domon US Publication No. 2003/0014679 A1.

Referring to claim 1, Stallkamp discloses, a data conversion system comprising:

a first and second node in which one of the first and second node (A/V devices 108 and 110, Stallkamp Fig. 1) on an IEEE1394 bus (isochronous network 104 is IEEE 1394 compliant, Stallkamp, column 4, lines 56-60) serves as a cycle master (Master 106, Stallkamp Fig. 1), the first node having a DV data processing unit (A/V devices 108 and 110 is equipped to generate and record digital video images in addition to recording

associated audio signal, see Col. 3, lines 13-19; also note A/V devices includes processor to process data signals, see Col. 3, lines 57-67), the second node being having a data conversion unit (frame rate converter for handling video data, see Col. 5, lines 58-67) configured to receive the first image data from the DV data processing unit of the first node via the IEEE1394 bus, convert the first image data to second image data by synchronizing second image data (synchronizing of video data, see Col. 1, lines 17-22) generated by the conversion of the first image data in the second node with an external reference signal (house reference signal 225, Stallkamp Fig. 2), the second node to output the second image data via the data conversion unit,

an external synchronizing signal receiver (SYNC 254, Stallkamp Fig. 2) for receiving the external reference signal (house reference signal 225, Stallkamp Fig. 2) provided on at least one of the first and second nodes (the house reference signal is provided to each node by the bus 102, Stallkamp Figs 1 and 2),

a synchronization adjustment unit for synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external reference signal received by the external synchronizing receiver, by carrying out feedback control of a clock source frequency (The synchronizer utilizes a feedback loop 401 to generate a locked cycle time, column 6, lines 30-43) of the cycle master using the external reference signal (Synchronizer 254 synchronizes the operating frequencies of AV devices and enables data based in one time domain to be transmitted over an isochronous bus of a second time domain, Stallkamp column 5, lines 10-20).

It is noted that Stallkamp does not appear to explicitly disclose, the first node being configured to transmit first data to the second node at a transfer rate synchronized with a cycle start packet output from the cycle master.

However, Domon discloses, the first node being configured to transmit first data (Digital Video data is mapped into isochronous packets and received by a digital video player 220, Domon page 6, paragraph 0098 lines 3-8 and paragraph 0099, lines 1-3) to the second node at a transfer rate synchronized with a cycle start packet output from the cycle master (the cycle master outputs a cycle start packet to the other nodes in the network to synchronize them to the master, Domon page 1, paragraph 0017, lines 1-5),

Stallkamp and Domon are analogous art because they are from the same field of endeavor, namely, they both synchronous video data transmitted over an IEEE 1394 bus.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Stallkamp and Domon before him or her, to enhance the communication and conversion methods of Domon with the synchronization with the house reference signal of Stallkamp.

The suggestion/motivation for doing so is present in Stallkamp, column 1 lines 59-67, where it states that A/V data may have been generated based on a clock and rate different from that of the isochronous bus used to transmit it and therefore the house reference signal with allow synchronization with both clock rates.

Therefore it would have been obvious to combine Domon with Stallkamp to obtain the invention as recited in the instant claim.

As per claim 2, it is noted that Stallkamp does not appear to explicitly disclose, the first data and the second data are image data, and the first data is a video signal in DV format and the second data is an analog video signal or SDI video signal.

However Domon discloses, the first data and the second data are image data, and the first data is a video signal in DV format and the second data is an analog video signal or SDI video signal (the digital video player 220 decodes the DV format data and outputs an analog video signal, Domon page 6, paragraph 0098, lines 6-8).

Stallkamp and Domon are analogous art because they are from the same field of endeavor, namely, they both synchronous video data transmitted over an IEEE 1394 bus.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Stallkamp and Domon before him or her, to enhance the communication and conversion methods of Domon with the synchronization with the house reference signal of Stallkamp.

The suggestion/motivation for doing so is present in Stallkamp, column 1 lines 59-67, where it states that A/V data may have been generated based on a clock and rate different from that of the isochronous bus used to transmit it and therefore the house reference signal with allow synchronization with both clock rates.

Therefore it would have been obvious to combine Domon with Stallkamp to obtain the invention as recited in the instant claim.

As per claim 3, the first node serves as cycle master for data transfer (AV devices 108 and 110 may function as the cycle master and maybe a device such as a digital video camera, Stallkamp column 3, lines 17-19 and 37-41).

As per claim 4, Stallkamp discloses, the second node comprises a second synchronization adjustment unit (SYNC 254, Stallkamp Fig. 2),

the frequency of the cycle start packet is linked with the frequency of the reference signal (Synchronizer 254 synchronizes the operating frequencies of AV devices and enables data based in one time domain to be transmitted over an isochronous bus of a second time domain, Stallkamp column 5, lines 10-20) by the synchronization adjustment unit of the node that serves as the cycle master (Either AV node 108 or AV node 110 may serve as cycle master, column 3, lines 37-41) (Therefore the second node, node, whether 108 or 110, may serve as the cycle master and synchronize itself internally).

As per claim 13, it is noted that Stallkamp does not appear to explicitly disclose, the first node is hardware comprising an 13940HCI compliant IEEE1394 interface for outputting a video signal in DV format as first data, and the second node is data conversion hardware for outputting an analog video signal or SDI video signal as second data.

However, Domon discloses, the first node is hardware comprising an 13940HCI compliant IEEE1394 interface for outputting a video signal in DV format as first data,

and the second node is data conversion hardware for outputting an analog video signal or SDI video signal as second data (the digital video player 220 decodes a digital video signal of DV format received from the IEEE1394 bus and outputs an analog video signal, Domon page 6, paragraph 0098, lines 6-8).

Stallkamp and Domon are analogous art because they are from the same field of endeavor, namely, they both synchronous video data transmitted over an IEEE 1394 bus.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Stallkamp and Domon before him or her, to enhance the communication and conversion methods of Domon with the synchronization with the house reference signal of Stallkamp.

The suggestion/motivation for doing so is present in Stallkamp, column 1 lines 59-67, where it states that A/V data may have been generated based on a clock and rate different from that of the isochronous bus used to transmit it and therefore the house reference signal with allow synchronization with both clock rates.

Therefore it would have been obvious to combine Domon with Stallkamp to obtain the invention as recited in the instant claim.

As per claim 14, Stallkamp discloses, the second node comprises the external synchronizing signal receiver and synchronization adjustment unit (both nodes receive the house reference clock 102, and contain a Sync unit 254, Fig. 2), and serves as cycle master for data transfer (column 3, lines 36-42).

As per claim 15, Stallkamp discloses, the first node comprises the synchronization adjustment unit, the second node comprises the external synchronizing signal receiver and synchronization adjustment unit (both nodes receive the house reference clock 102, and contain a Sync unit 254, Fig. 2),

It is noted that Stallkamp does not appear to explicitly disclose, the cycle start packet frequency is synchronized with the frequency of the external reference signal received by the external synchronizing signal receiver by means of the synchronization adjustment unit of the node that serves as cycle master.

However, Domon discloses, the cycle start packet frequency is synchronized with the frequency of the external reference signal received by the external synchronizing signal receiver by means of the synchronization adjustment unit of the node that serves as cycle master (the cycle master outputs a cycle start packet to the other nodes in the network to synchronize them to the master, Domon page 1, paragraph 0017, lines 1-5),

Stallkamp and Domon are analogous art because they are from the same field of endeavor, namely, they both synchronous video data transmitted over an IEEE 1394 bus.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Stallkamp and Domon before him or her, to enhance the communication and conversion methods of Domon with the synchronization with the house reference signal of Stallkamp.

The suggestion/motivation for doing so is present in Stallkamp, column 1 lines 59-67, where it states that A/V data may have been generated based on a clock and rate different from that of the isochronous bus used to transmit it and therefore the house reference signal with allow synchronization with both clock rates.

Therefore it would have been obvious to combine Domon with Stallkamp to obtain the invention as recited in the instant claim.

As per claim 16, Stallkamp discloses, when the first node serves as cycle master, the external reference signal received by the external synchronizing signal receiver of the second node is transmitted from the second node to the first node by asynchronous transfer of an IEEE 1394 interface (column 3, lines 50-54).

As per claim 17, Stallkamp discloses, a dedicated synchronization signal line for transmitting the external reference signal received by the external synchronizing signal receiver of the second node from the second node to the first node when the first node serves as cycle master (House reference clock 102, Figs 1 and 2).

As per claim 18, Stallkamp discloses, the first node comprises the external synchronizing signal receiver ad synchronization adjustment unit (both nodes receive the house reference clock 102, and contain a Sync unit 254, Fig. 2), and serves as cycle master for data transfer (column 3, lines 36-42).

As per claim 19, Stallkamp discloses, one of the first node and the second node serves and the cycle master (column 3, lines 36-42) and the other of the first node and the second node includes the synchronization adjustment unit (both nodes receive the house reference clock 102, and contain a Sync unit 254, Fig. 2).

Note claims 20 and 21 recite the corresponding limitations of claims 1 and 2. Therefore they are rejected based on the same reason accordingly.

Response to Arguments

Applicant's arguments filed on 7/15/2011 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not

in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

Applicants argued that "Stallkamp does not teach the synchronizer 254 directly communicating with isochronous transport medium 104." (Page 7, 1st para. of Amendment)

Examiner does not agree with Applicants. As set forth in the art rejections, Stallkamp in view of Domon discloses the first node having a DV data processing unit (A/V devices 108 and 110 is equipped to generate and record digital video images in addition to recording associated audio signal, see Col. 3, lines 13-19; also note A/V devices includes processor to process data signals, see Col. 3, lines 57-67), the second node being having a data conversion unit (frame rate converter for handling video data, see Col. 5, lines 58-67) configured to receive the first image data from the DV data processing unit of the first node via the IEEE1394 bus, convert the first image data to second image data by synchronizing second image data (synchronizing of video data, see Col. 1, lines 17-22) generated by the conversion of the first image data in the second node with an external reference signal (house reference signal 225, Stallkamp Fig. 2), the second node to output the second image data via the data conversion unit. Nowhere in the claim does it mention that a synchronizer needs to directly communicate with an isochronous transport medium. In addition, the term "data" is defined as items of information and thus any signal (such as a reference signal, a clock signal, etc.) or timestamp information involving the images or video may be interpreted as "image

data". Applicants are suggested to specify the image data and to clarify the path of the data conversion.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In summary, Stallkamp and Domon teach the claimed limitations as set forth.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Titus Wong whose telephone number is **(571) 270-1627**. The examiner can normally be reached on Monday-Friday, 10am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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